What is Claimed is:

[c1] 1. A system for dynamically altering a clock speed of a clock signal used for timing of data signal transmissions and receptions within an integrated circuit (IC) device comprising: a clock generator circuit for providing said clock signal used for timing of data signal transmission and reception within said IC; a monitoring circuit means for receiving data transmissions generated at different clock speeds and detecting when a data transmission fail point is achieved at a particular clock speed; and, means for adjusting said clock speed according to a maximum speed allowed for the IC that avoids said data transmission fail point.

[c2] 2. The system as claimed in Claim 1, wherein said means for adjusting comprises means for generating a feedback control signal for input to said clock generator circuit for adjusting said clock to said maximum speed.

[c3] 3. The system as claimed in Claim 1, wherein said clock generator circuit comprises a multiplexor device comprising one or more clock taps responsive to said feedback control signal for enabling alteration of said clock speed.

[c4] 4. The system as claimed in Claim 2, further comprising: an error correction signal generating circuit for generating error correction signals according to each data signal transmission, said monitoring circuit comprising including an error correction signal check circuit for receiving said error correction signals and comparing error correction signals generated at each clock speed against known error corrections corresponding to each data transmission, wherein a data transmission fail point corresponds to a clock speed resulting in an error between said error correction signals and said corresponding known error corrections.

[c5] 5. The system as claimed in Claim 2, further comprising: a means for delaying each of a series of data transmission signals generated at different clock speeds; said monitoring circuit comprising including an error check circuit for receiving each of said series of delayed data transmission signals and comparing each delayed data transmission signal against a corresponding known data signal transmission, wherein a data transmission fail point corresponds to a clock speed resulting in an error between said delayed data

transmission signal and said corresponding known data transmission.

[c6] 6. The system as claimed in Claim 2, further comprising: a random data generating circuit for generating unique random data transmission signals for input to said IC device, said IC device for processing said random data in and generating a corresponding data output; said monitoring circuit including a means for comparing said generated random data against said corresponding data output of said processing circuit, wherein a data transmission fail point corresponds to a clock speed resulting in an error between said generated random data and said corresponding processing circuit output.

[c7] 7. The system as claimed in Claim 6, wherein said comparator means generates said feedback control signal indicating said data output of said processing circuit matches said generated random data, said feedback control signal being input to said clock generator circuit for enabling the clock frequency provided by clock generator circuit to be increased.

[c8] 8. The system as claimed in Claim 6, wherein said comparator means generates said feedback control signal indicating said data output of said processing circuit does not match said generated random data, said feedback control signal being input to said clock generator circuit for enabling the clock frequency provided by clock generator circuit to be decreased.

[c9] 9. The system as claimed in Claim 6, wherein said random data generating circuit includes a random number generator for receiving a seed value and generating said unique random data therefrom.

[c10] 10. The system as claimed in Claim 5, wherein said means for delaying each of a series of data transmission signals comprises means for increasing a load applied to data lines carrying said data transmission signals to said error check circuit.

[c11] 11. A method for dynamically altering a system clock speed regulating data signal transmission and receptions in an Integrated Circuit (IC), said method comprising the steps of: a) providing said clock signal used for timing of data signal transmission and reception within said IC; b) receiving data transmissions

generated at different clock speeds and detecting when a data transmission fail point is achieved at a particular clock speed; and, c) adjusting said clock speed according to a maximum speed allowed for the IC that avoids said data transmission fail point.

[c12] 12. The method as claimed in Claim 11, wherein said adjusting step c) includes the step of generating a feedback control signal for input to said clock generator circuit, said feedback signal for adjusting said clock to said maximum speed.

[c13] 13. The method as claimed in Claim 12, further comprising the steps of: generating error correction signals according to each data signal transmission, receiving said error correction signals and comparing error correction signals generated at each clock speed against known error corrections corresponding to each data transmission, wherein a data transmission fail point corresponds to a clock speed resulting in an error between said error correction signals and said corresponding known error corrections.

[c14] 14. The method as claimed in Claim 12, further comprising the steps of: delaying each of a series of data transmission signals generated at different clock speeds; receiving each of said series of delayed data transmission signals and comparing each delayed data transmission signal against its corresponding known data signal transmission, wherein a data transmission fail point corresponds to a clock speed resulting in an error between said delayed data transmission signal and said corresponding known data transmission.

[c15] 15. The method as claimed in Claim 12, further comprising the steps of: generating unique random data transmission signals; transmitting said unique random data signals to said IC device for processing therein, and generating a corresponding data output signal; and, comparing said generated random data against said corresponding data output of said processing circuit, wherein a data transmission fail point corresponds to a clock speed resulting in an error between said generated random data and said corresponding processing circuit output.

[c16] 16. The method as claimed in Claim 12, wherein said feedback control signal includes a first signal indicating a match between said data output signal of said data path and said generated unique random data, or generating a second output signal indicating no match between said data output signal of said data path and said generated unique random data, wherein said adjusting step c) includes responding to either said first or second output signals for respectively increasing or decreasing a clock frequency of said clock signal.

[c17] 17. The method as claimed in Claim 14, wherein said delaying step includes the step of increasing a load applied to data lines carrying said data transmission signals to said error check circuit.

[c18] 18. The method as claimed in Claim 12, further including the step of continuously detecting presence of data transmission fail points to ensure that the errors do not occur as the IC incurs different operating conditions, said monitoring including adjusting the clock speed accordingly.